

Review of Transputer Hardware and System Design by Jeremy Hinton and Alan Pinder

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The reviewed book is intended as a practical guide to transputer hardware design. The authors do not assume prior knowledge of the transputer architecture, but the reader should be familiar with more conventional micro-processor design.

Transputers are a family of micro-processors created by INMOS, now owned by SGI Thompson. Transputers are fast RISC processors that were especially designed to facilitate simple single-processor as well as multi-processor designs. To achieve the first goal, transputers are highly integrated (computers on a chip); they include an external memory interface (S/D-RAM controller) and internal memory. Transputers can operate when connected solely to power and a clock signals, since four high speed serial links can provide IO. These links can also be used to connect multiple transputers and the instruction set has built-in multi-tasking support. These two features simplify the design of multi-processor systems.

The book gives a brief introduction to transputer architecture, focusing on its novel features. For example, the parallel programming support for processes and inter-process communication, which is based on the communicating sequential programming (CSP) model by Hoare. Chapter two gives a brief introduction to the transputer's instruction set.

There are two different types of external memory interfaces available, one that supports fast static RAM (two-cycle) and one that is programmable and is mainly intended for slower dynamic memory (three-cycle).

Chapters three and four describe the two-cycle memory interface. The two-cycle memory interface uses separate data and address busses. Therefore, it is only supported on the 16-bit transputers and on a special version (T801) of the 32-bit processors. Chapter four includes three design examples: a 62256 SRAM, a DAC (AD667), and a ADC (AD7572) interface.

The three-cycle memory interface described in chapter five is intended for DRAM systems and other complex memory mapped IO devices. The address and data busses are

multiplexed to reduce the number of pins. The three-cycle external memory interface contains several programmable strobe signals that can be used to create chip select, output enable, or row/column address signals. Furthermore, the refresh is fully supported on chip. Therefore, all that is required to connect up to 2 MB of DRAM to a transputer are address latches to de-multiplex the data and address busses. Chapter six contains design examples for slow SRAM, DRAM, and combined DRAM/ROM systems.

Chapter seven covers transputer interconnections. Although shared memory systems are possible, the transputer model assumes that each processor contains only local resources (memory, disk drives, etc.) and all interconnections are done using the on-chip links. INMOS offers two link adaptor chips that allow to connect transputers to other processors (C012 or C011 Mode 2) or to parallel ports (C011 Mode 1). Chapter seven also introduces the C004 programmable interconnection chip, which allows flexible inter-processor connections. The chapter covers interfacing to an ADC using a link adaptor chip (C011) and some very general information on how to connect a link adaptor to the PC ISA bus.

Since debugging and testing multi-processor system is inherently more complex than sequential computer systems, the authors dedicated chapter eight to the debugging facilities of the transputer. Transputers provide special signal that allows postmortem debugging, peek, and poke of transputer networks. However, debugging transputer system is only considered in the context of system testing. Readers interested in tracking bugs in application programs will be disappointed.

Chapter nine describes the next generation of transputers, the T9000. This new transputer chip has been advertised for a year, but has not been available yet and the information in the book is preliminary. Therefore, the T9000 chapter does not include sufficient information for T9000 design. It is more of descriptive than practical design value.

INMOS made significant improvements to the transputer architecture mainly in three areas: speed, memory interface, and link engine. The T9000 is expected to run at 200 MIPS peak performance. The internal memory can be used as either standard memory or cache. The external memory interface is more flexible. Address translation and protection provide, albeit incomplete, virtual memory support. Another important improvement is the complete redesign of the link engine, which now has built-in virtual channel support.

The appendix contains some excerpts from the transputer data sheets, PAL design equations for some of the design examples, and some sample programs for system testing. The book also contains an adequate index and bibliography sections.

It is the opinion of this reviewer that much information presented in this book is available in more detail elsewhere, for example the transputer data sheets and the INMOS OCCAM 2 reference manual. This is particularly true for the introductory chapters covering the parallel processing model (Processes, Channels, OCCAM) and the transputer architecture. However, the chapters covering the two-cycle (chapters 3,4) and three-cycle memory (chapters 5,6) interfaces are useful, since they cover different design possibilities and do include some practical tips and pitfalls of transputer system design.

Overall, the book can be recommended for people as a good starting point, but readers should not expect a complete design without additional information.